A Method for Troubleshooting Noise Internal to an IC

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Abstract: A method for measuring internal noise in an IC package and its external manifestations is presented. Typical measured data are shown. Use of this measurement method can significantly increase the probability that a new or modified design is reliable, able to be manufactured, and meets EMC requirements. In addition, EMC and design problems resulting from internal chip noise can be found and fixed faster and at less expense than possible using more conventional methods.

Introduction

Many engineers have had the experience of retrofitting a new IC to replace an IC of an older technology in an existing design only to have the circuit fail to function reliably or cause an EMC problem. Often such a fault is discovered after the older part is no longer available.

With the high level of complexity in today's digital circuits it is difficult to determine that a circuit is working exactly as intended. When a problem does occur, high performance logic analyzers and other expensive equipment maybe necessary to find the problem if it is due to internal chip noise. The equipment is not only expensive and potentially not available when needed, but large amounts of engineering time can be spent tracking down the problem.

The method presented here uses only a digitizing oscilloscope with a one or two gigasample per second digitizing rate, a good set of probes, and a pickup loop that can be made from a paperclip.

Problem Description

Internal chip noise can manifest itself as glitches on chip outputs. Sources of these glitches can include ground bounce on the die and crosstalk between wirebonds. Unfortunately, these two modes of noise generation can add in phase to make the problem worst. An example of how this can happen is shown in Figure 1.

Figure 1 shows the outline of an 84 pin package with only the pins of interest to this discussion shown. Assume that an output on pin 74 is being held low by the chip while the chip is driving pin 75 from high to low. To do that, current must be pulled into pin 75 and sent to a ground pin as shown. This creates an inductive voltage drop (L·di/dt) across the ground bonding wire in the package as shown in Figure 1. The chip die is raised above ground by the inductive drop across the ground lead and a positive pulse occurs on pin 74 due to the die voltage rise. This is classical ground bounce.

Crosstalk from pin 75 to 74 will add to the ground bounce seen on pin 74. The current flowing into pin 75, as it is pulled low, also creates an inductive voltage drop across its bond wire of the polarity shown, + towards pin 75 and - towards the chip die. This creates a mutual inductive voltage drop in the bonding wire of pin 74 of the same polarity as the bonding wire on pin 75.

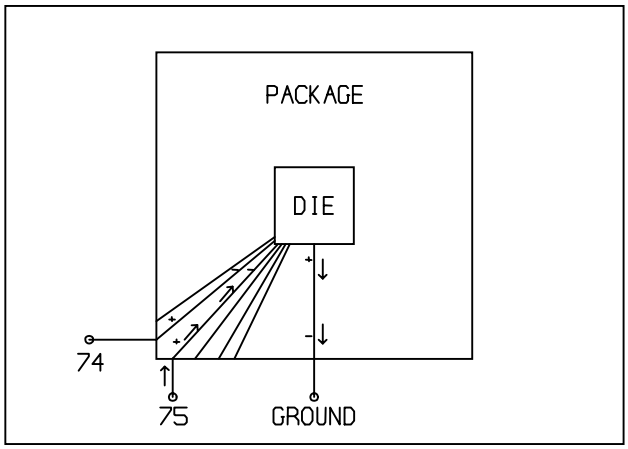

Figure 1. Chip/Package Noise Voltages.

Its magnitude (M·di/dt) will be lower than the inductive drop across pin 75's bonding wire. In this case, the mutual inductance, M, could be on the order of 1/3 of the inductance of the adjacent bonding wire of pin 75.

The total "ground bounce" seen on pin 74 can be the real ground bounce due to the current flowing in the ground lead ***plus*** the mutually inductive crosstalk from pin 75. This can happen at times when the ground bounce is at least partially due to the low going signal on pin 75. If an output on pin 73 also had a low going signal at the same time, the crosstalk could potentially be doubled.

The combination of low going signals on different pins combined with crosstalk into the pin of interest can cause problems that occur with a low repetition rate. Often, minutes can lapse between hits.

If a logic analyzer is used to trigger on an error condition, the nanosecond wide glitch that caused it may be

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milliseconds back in time. This requires the logic analyzer to have a very deep memory and fast clock rate. Both of which translate into a very expensive instrument.

Measurement Method

The method has two parts. Construction of a pickup loop and use of a scope probe to look at signals on the pins of the IC.

Loop Construction

A square loop is constructed so that a side has the same length as the distance from the center of the chip to a corner. This loop generally does not need to be shielded and can be constructed from any stiff wire, a bent paperclip works well [1]. The wire should be covered with thin insulation such as spaghetti tubing. A round shielded loop of the type used for EMC investigations will work, but generally will be less sensitive than a square loop which captures more of the magnetic flux generated by the chip die and package.

The pickup loop should be connected through a length of 50 ohm coaxial cable to the 50 ohm input of the digitizing oscilloscope. During use it is held perpendicular to the chip.

Procedure

The digitizing oscilloscope is set up with two traces, one for the pickup loop and the second for a scope probe. It is best to use a high performance FET or Balanced Coaxial Probe and keep lead lengths to less than an inch [2]. The scope should be triggered from the pickup loop.

Typical scope parameters are 2 volts per division for the probe and 200 mv per division for the pickup loop. 10 ns per division is a good starting point for the horizontal sweep rate.

The pickup loop is placed perpendicular to the chip package with one corner at the center of the chip and the other corner at the edge of the package. The loop is then rotated slowly over 360^{o}, holding one corner at the center of the package. The orientation of the loop is noted at those locations where more than 50 mv peak is displayed on the scope.

Keep in mind that the mutual inductance between the loop and bonding wires in the chip package is less than the inductance of the bonding wires. Therefore, the loop output (M·di/dt) represents a lower bound of the inductive drop across the bonding wires (L·di/dt) and has the same waveshape. It is reasonable to expect that M is about 0.25L, although considerable variation is possible. The loop output also represents an estimate of crosstalk into nearby bonding wires from current flowing in the bonding wire directly under the loop.

At each location where the loop output is significant, greater than 50 mv, fix the loop at that position and using the scope probe look at each signal output of the chip. Sometimes the results can be surprising.

Results

Figure 2 shows the result of one such measurement. Due to differences in time delay between the FET probe, upper trace, and the pickup loop, lower trace, there is an extra 1 to 2 ns of delay in the upper trace. The second peak of the loop output on the lower trace should line up with the "glitch" seen by the FET probe.

Note that the amplitude of the loop output goes well past minus 100 mv indicating that a bonding wire inside the package probably has on the order of 500 mv of inductive drop across it! Only the second positive peak of the loop output manifests itself in the probed output of the chip. This is because the output waveform was low during the second peak.

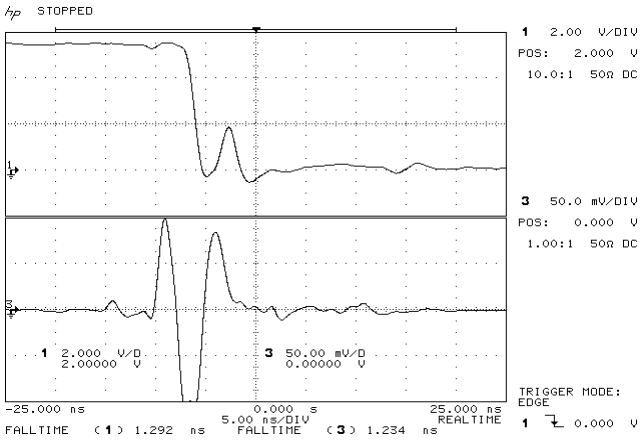

Figure 2. Measurement Example 1.

The upper trace waveform shown in Figure 2 was clearly a problem since it was an edge triggered signal. It "bounces" up to almost two volts above ground!

A second example is shown in Figure 3. In this case, after the pickup loop identified a problem on a bonding wire, a probe was placed on the signal corresponding to that bonding wire. The signal is displayed on the lower trace.

It was subsequently determined that a race in the chip caused a "glitch" on that lead (probe signal on the lower trace) which coupled though both crosstalk and ground bounce into a low going signal on an adjacent pin (probe signal on the upper trace). Note that it is during the falling edge of the glitch that the peak of the ground bounce occurs in the low going signal. At that time, L·di/dt drop is being generated across the chip ground bonding leads and also crosstalk (M·di/dt) is occurring on adjacent bonding leads.

If such a "glitch" occurs with a low frequency, say once per minute, finding it can present a problem. The troubleshooting process is even more complex if the glitch precedes the observable result by milliseconds. Normally, a logic analyzer would have to be used that samples every nanosecond for milliseconds to look back from the observable problem in the circuit to the glitch. This implies a

very long memory in the analyzer and a very high cost of the instrument.

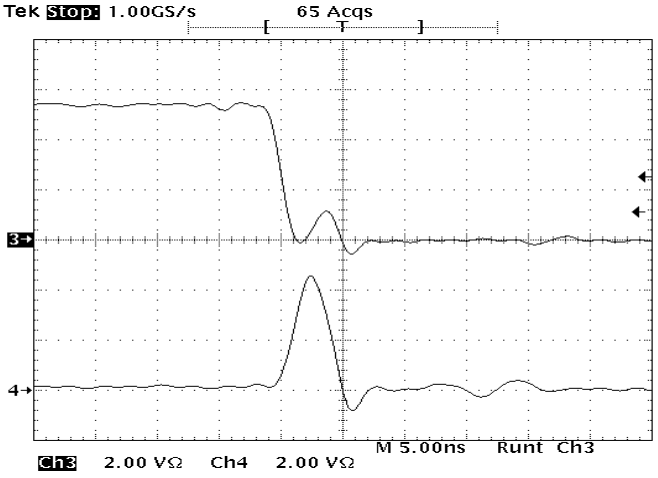

Figure 3. Measurement Example 2.

Figure 4 shows another measurement. In this measurement, the loop output is on the lower trace and a signal is measured with an FET probe. As in Figure 2, the top trace is delayed about 1 or 2 nanoseconds from the bottom trace because of the different delays of the probe and pickup loop.

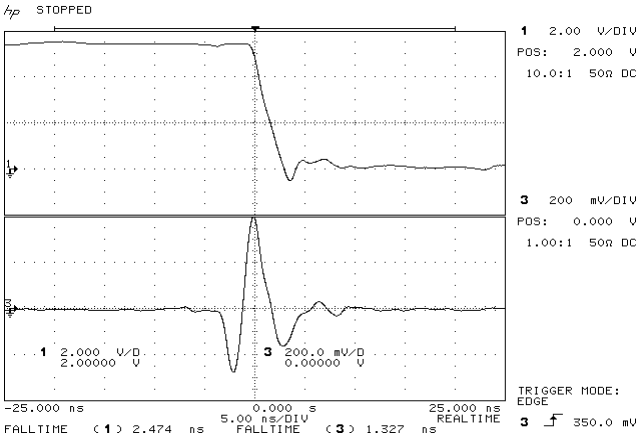

Figure 4. Measurement Example 2.

The large positive spike in the loop output occurs during the falling edge of the signal. This causes the falling edge to break to a slower slew rate about 1/3 down on the falling edge. This would probably not be a problem for most circuits. However, if the positive spike were delayed another 5 nanoseconds, it would result in a signal similar to the ones in Figures 2 and 3 having a discrete "glitch" after the falling edge.

The loop output voltage reaches about 400 mv peak! This means that the bonding wire under the loop may have a significant fraction of a volt of inductive drop across it. This much inductive drop can cause problems of its own in the chip in addition to "glitching" chip output signals.

If the traces of Figure 4 are displayed on the longer time scale of 200 ns/div, shown in Figure 5, one can see that the pulse picked up by the loop is a relatively rare event. The method of using the loop to find noise events, trigger the scope, and then looking at chip signals with a probe, works very well on this type of problem.

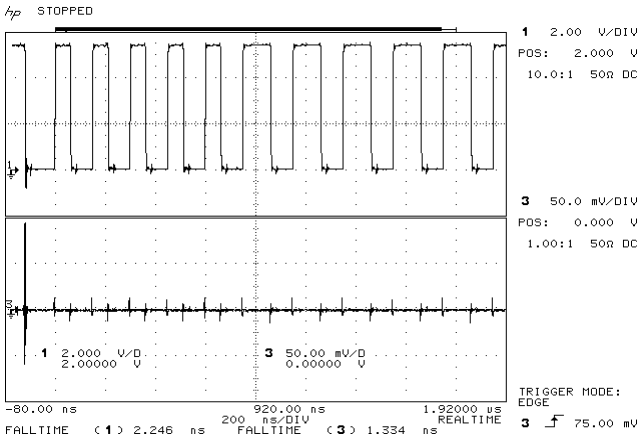

Figure 5. Measurement Example 3.

Summary and Conclusions

Ground bounce in an IC package can be additive with crosstalk. Crosstalk between bonding wires in the chip package can add 20% or so to existing ground bounce as seen on a low output signal.

The effect of ground bounce and crosstalk on output signals of a chip can be determined by using a square pickup loop and a scope probe. The loop is rotated on the top of the chip package to find bonding wires with significant inductive drop. For each case of loop pickup greater than 50 mv, a scope probe is used to measure each output signal of the chip with the scope triggered from the loop. The results of several measurement examples were presented.

This method has been used many times to successfully measure the effects of internal chip noise on a board. It can be extended to finding how chip noise manifests itself elsewhere in a system by moving the scope probe to other parts of the system. One possibility is to use a current probe on system cables to relate noise on a particular chip to noise on a given cable.

References

[1] *High Frequency Measurements and Noise in Electronic Circuits*, Douglas C. Smith, published by Van Nostrand Reinhold, Chapter 7, pp. 125-157.

[2] "Techniques and Methodologies for Making System Level ESD Response Measurements for Troubleshooting or Design Verification," Douglas C. Smith, 1992 EOS/ESD Symposium Proceedings, pp. 2.2.1-2.2.8